FIG.1

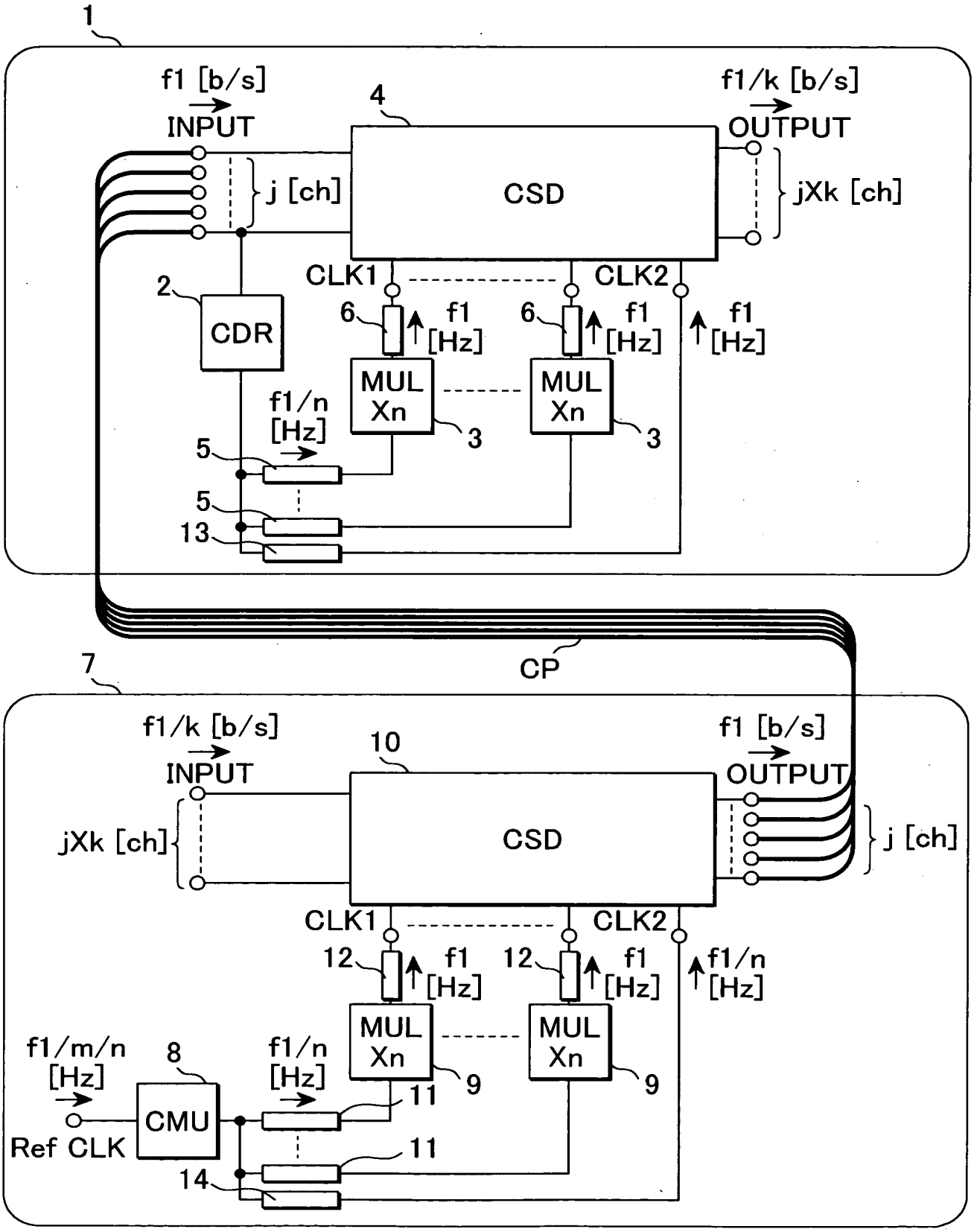

1
f1 [b/s]
INPUT
4
f1/k [b/s]
OUTPUT
j [ch]
CSD
jXk [ch]
CLK1
CLK2
2
CDR
6
f1 [Hz]
6
f1 [Hz]
f1 [Hz]
MUL Xn
3
MUL Xn
3
f1/n [Hz]
5
5
13
CP
7
f1/k [b/s]
INPUT
10
f1 [b/s]
OUTPUT
jXk [ch]
CSD
j [ch]
CLK1
CLK2
12
f1 [Hz]
12
f1 [Hz]
f1/n [Hz]
MUL Xn
9
MUL Xn
9
f1/m/n [Hz]
8
f1/n [Hz]
11
CMU
Ref CLK
11
14

FIG.2

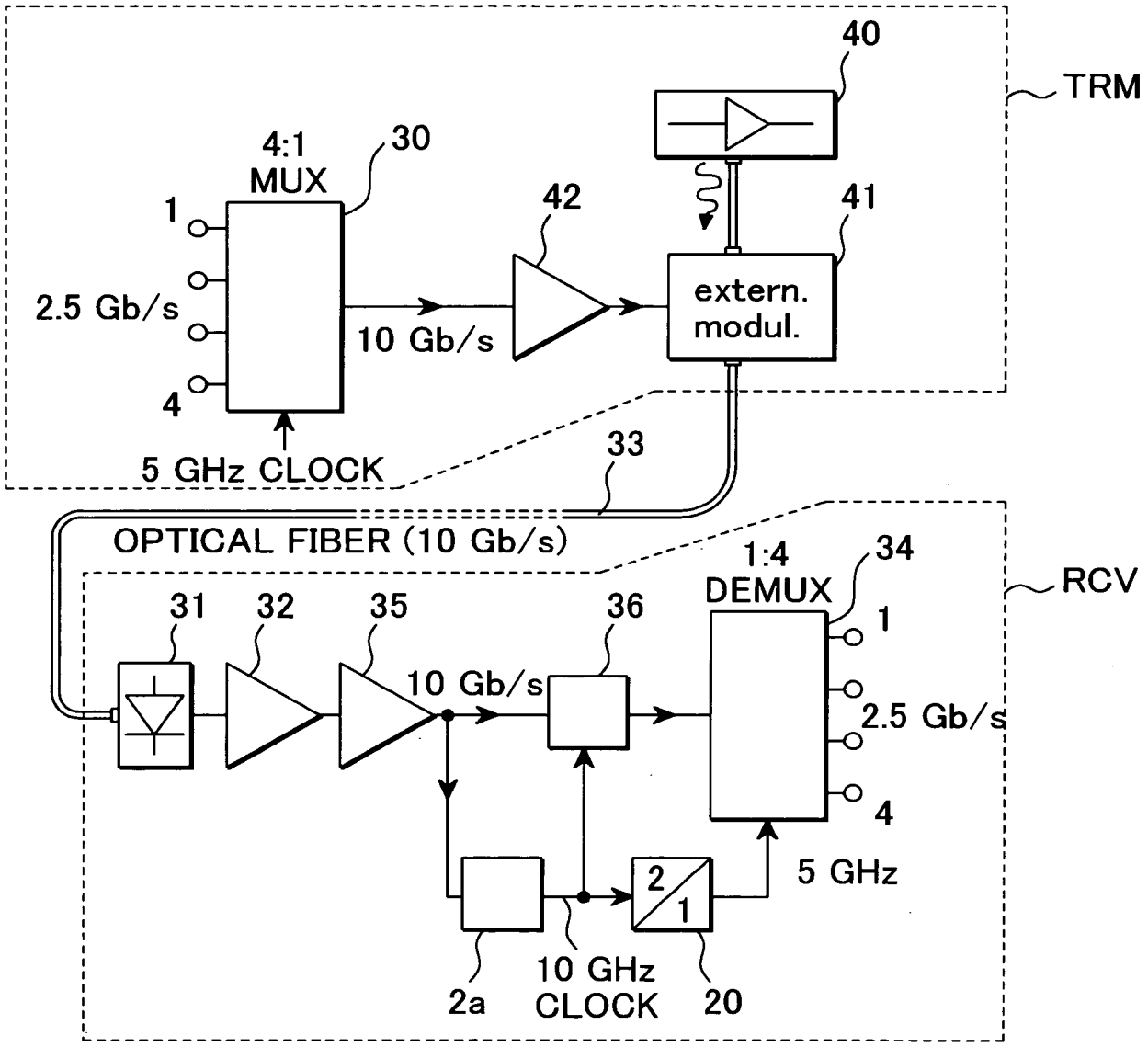

TRM
40
4:1
MUX
30
1
2.5 Gb/s
4
42
41
extern.
modul.
10 Gb/s
5 GHz CLOCK
33
OPTICAL FIBER (10 Gb/s)
RCV
1:4
DEMUX
34
31
32
35
36
10 Gb/s
1
2.5 Gb/s
4
5 GHz
2
1
2a
10 GHz
CLOCK
20

FIG.3

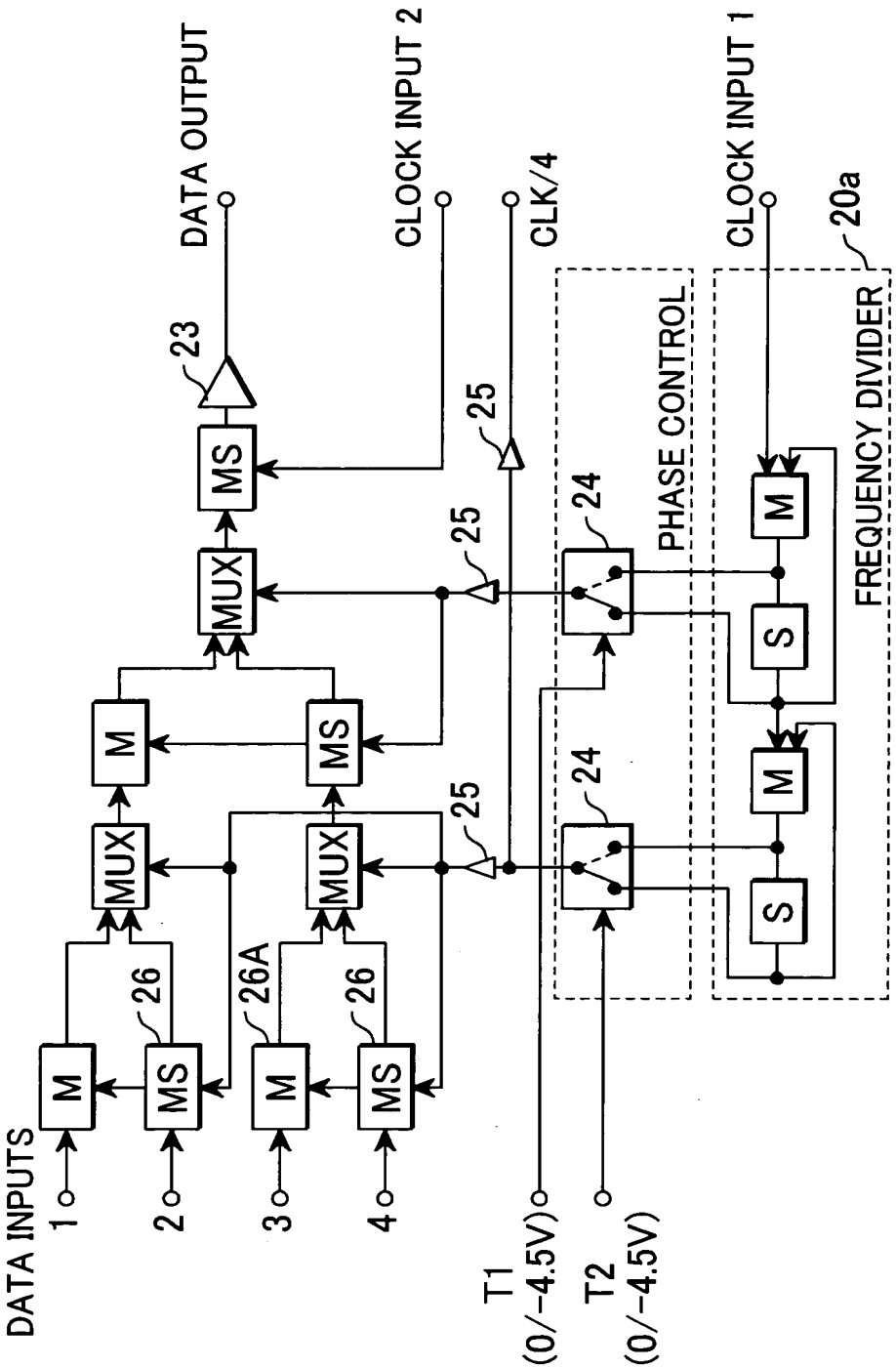

DATA INPUTS
1
2
3
4
M
MS
26
26A
MUX
M
MS
MUX
MUX
25
25
25
MS
23
DATA OUTPUT
CLOCK INPUT 2
CLK/4
T1
(0/−4.5V)
T2
(0/−4.5V)
24
24
PHASE CONTROL
CLOCK INPUT 1
M
S
M
S
20a
FREQUENCY DIVIDER

FIG.4

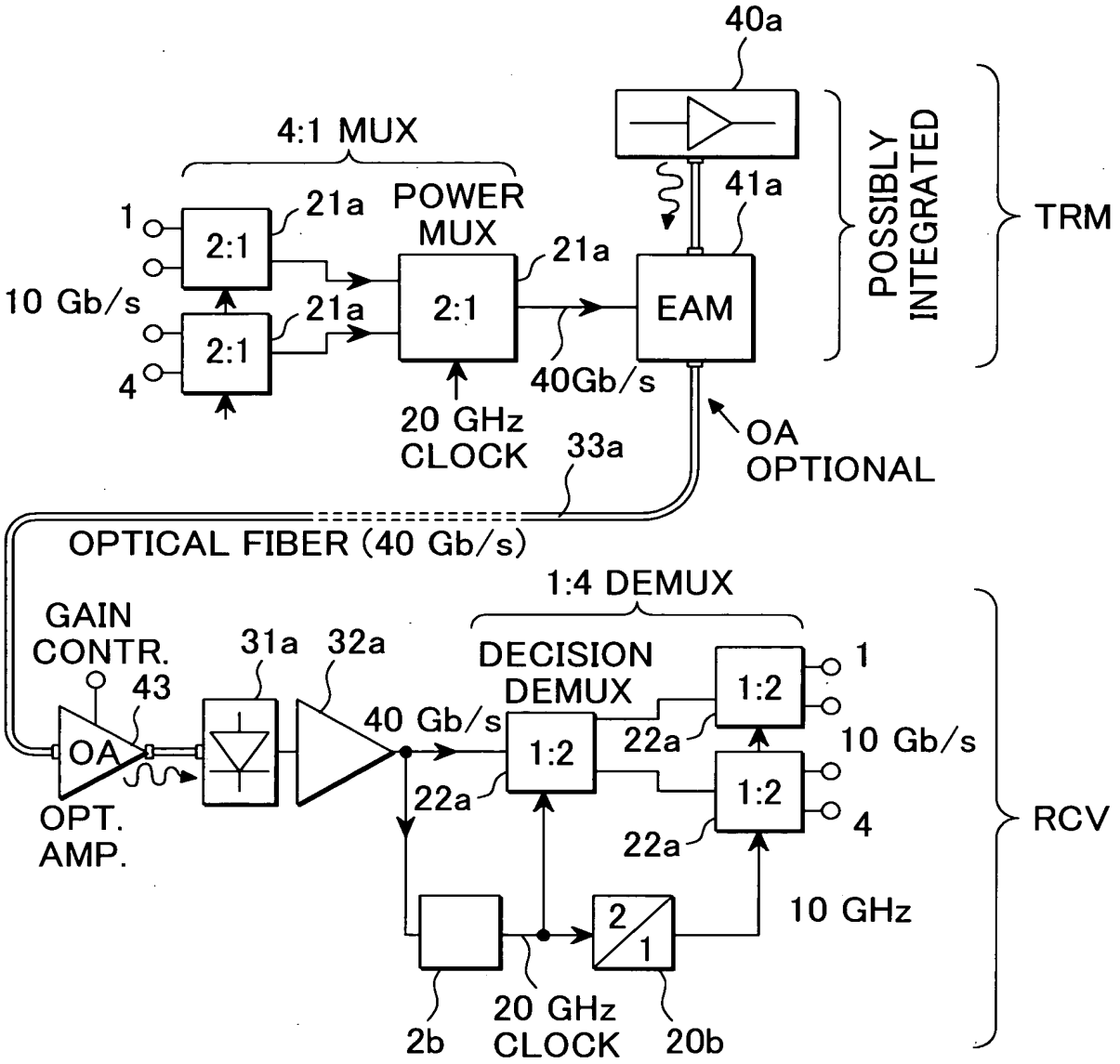

40a
4:1 MUX
POWER MUX
21a
41a
1
2:1
10 Gb/s
2:1
4
21a
2:1
21a
EAM
40Gb/s
20 GHz CLOCK
33a
OA OPTIONAL
POSSIBLY INTEGRATED
TRM
OPTICAL FIBER (40 Gb/s)
1:4 DEMUX
GAIN CONTR.
43
31a
32a
DECISION DEMUX
40 Gb/s
1:2
22a
1:2
1
10 Gb/s
OA
OPT. AMP.
22a
1:2
4
22a
RCV
10 GHz
2
1
2b
20 GHz CLOCK
20b

FIG.5

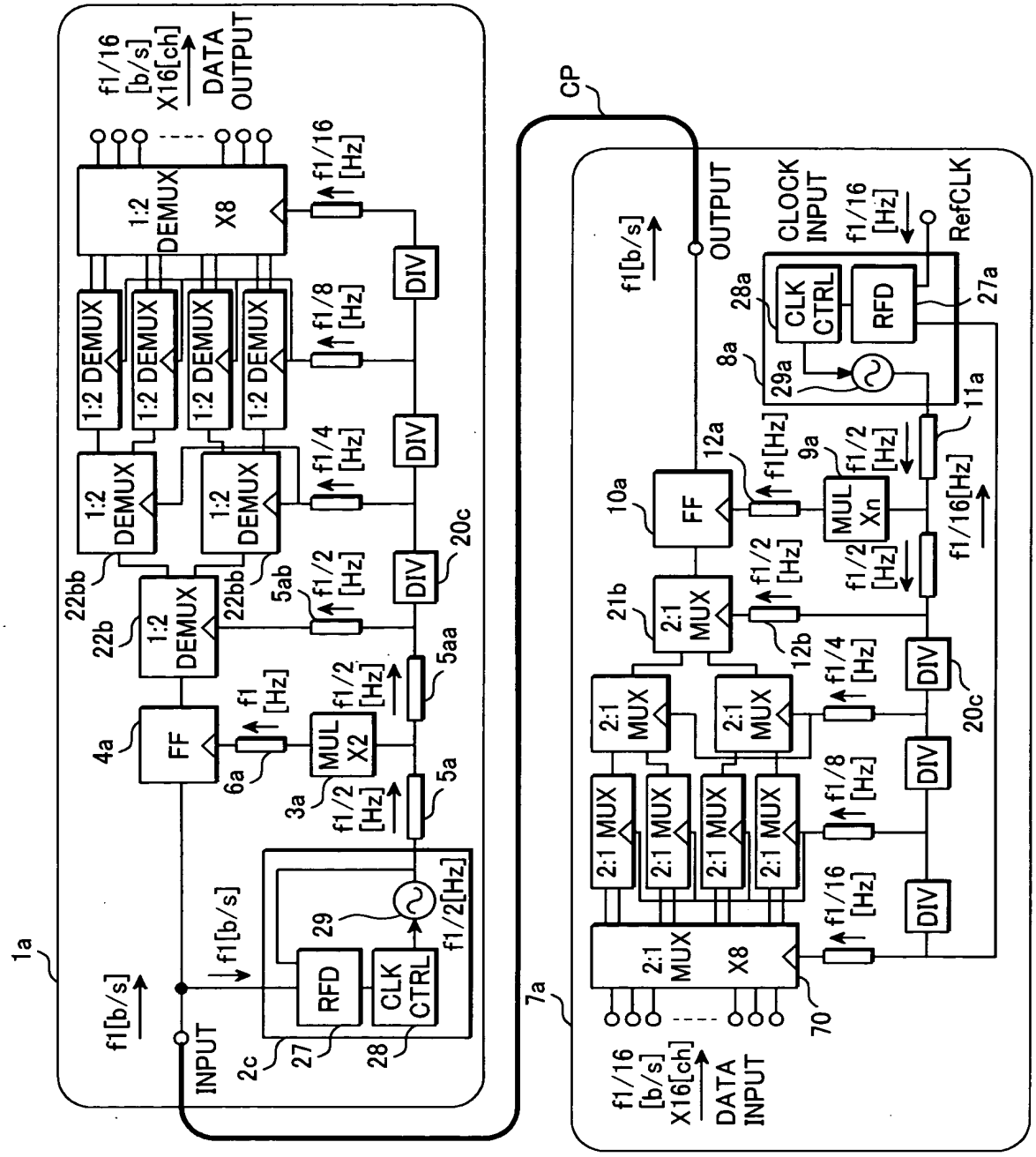

1a
f1[b/s]
INPUT
f1[b/s]
2c
RFD
27
CLK CTRL
28
29
f1/2[Hz]
3a
f1/2 [Hz]
MUL X2
6a
f1 [Hz]
4a
FF
22b
1:2 DEMUX
22bb
1:2 DEMUX
1:2 DEMUX
5ab
f1/2 [Hz]
5aa
5a
DIV
20c
f1/4 [Hz]
1:2 DEMUX
1:2 DEMUX
DIV
f1/8 [Hz]
1:2 DEMUX
1:2 DEMUX
1:2 DEMUX
1:2 DEMUX
DIV
f1/16 [Hz]
1:2 DEMUX
X8
f1/16 [b/s] X16[ch]
DATA OUTPUT
CP
7a
f1/16 [b/s] X16[ch]
DATA INPUT
70
2:1 MUX
X8
2:1 MUX
2:1 MUX
2:1 MUX
2:1 MUX
2:1 MUX
2:1 MUX
2:1 MUX
2:1 MUX
f1/16 [Hz]
DIV
f1/8 [Hz]
DIV
f1/4 [Hz]
DIV
20c
21b
2:1 MUX
12b
f1/2 [Hz]
10a
FF
12a
f1[Hz]
f1[b/s]
OUTPUT
f1/2 [Hz]
MUL Xn
9a
f1/2 [Hz]
f1/16[Hz]
CLOCK INPUT
f1/16 [Hz]
RefCLK
28a
CLK CTRL
RFD
27a
8a
29a
11a

FIG.6

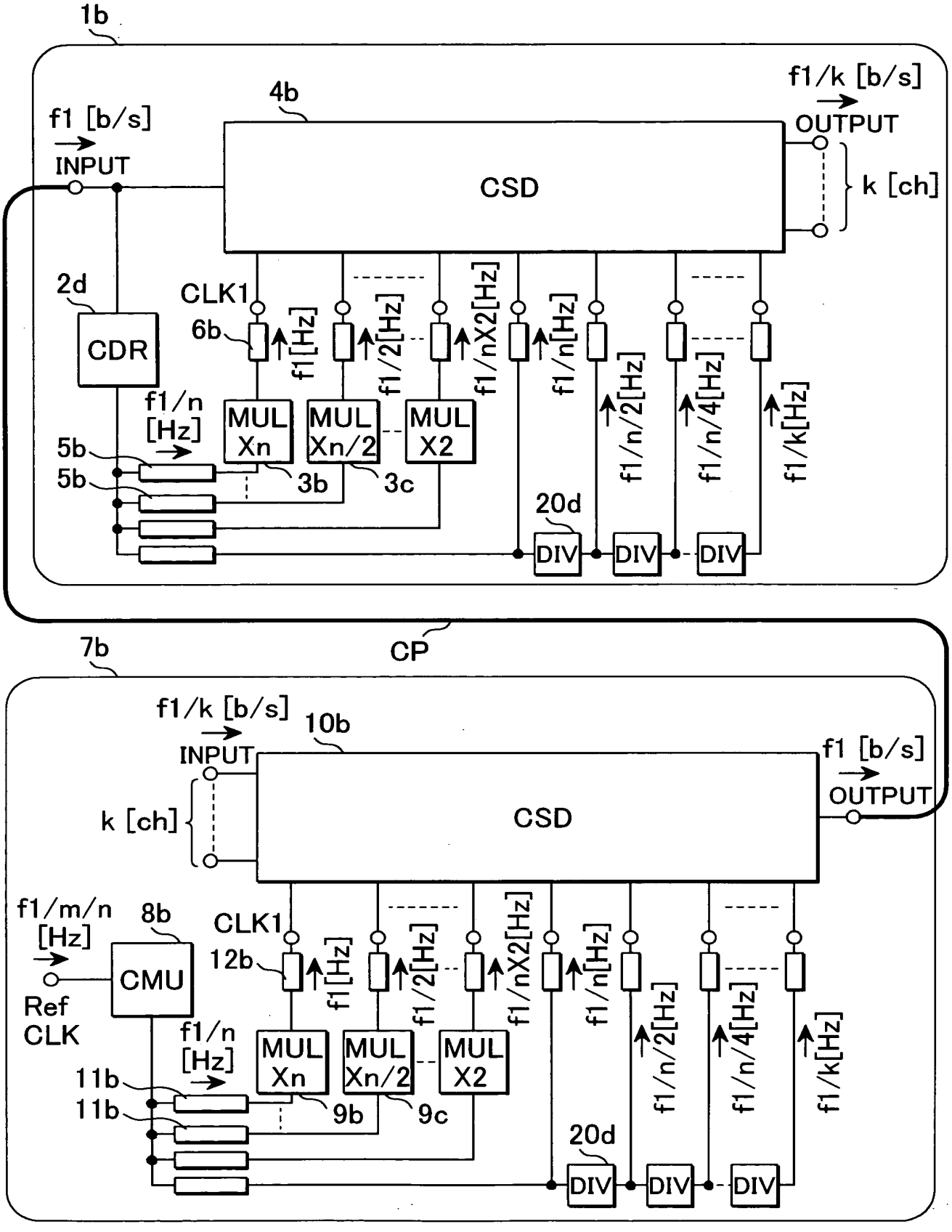

1b
f1/k [b/s]
OUTPUT
4b
f1 [b/s]
INPUT
CSD
k [ch]
2d
CDR
CLK1
6b
f1[Hz]
f1/2[Hz]
f1/nX2[Hz]
f1/n[Hz]
f1/n/2[Hz]
f1/n/4[Hz]
f1/k[Hz]
f1/n [Hz]
MUL Xn
MUL Xn/2
MUL X2
5b
5b
3b
3c
20d
DIV
DIV
DIV
CP
7b
f1/k [b/s]
INPUT
10b
f1 [b/s]
OUTPUT
k [ch]
CSD
f1/m/n [Hz]
8b
CMU
Ref CLK
CLK1
12b
f1[Hz]
f1/2[Hz]
f1/nX2[Hz]
f1/n[Hz]
f1/n/2[Hz]
f1/n/4[Hz]
f1/k[Hz]
f1/n [Hz]
MUL Xn
MUL Xn/2
MUL X2
11b
11b
9b
9c
20d
DIV
DIV
DIV

FIG.7

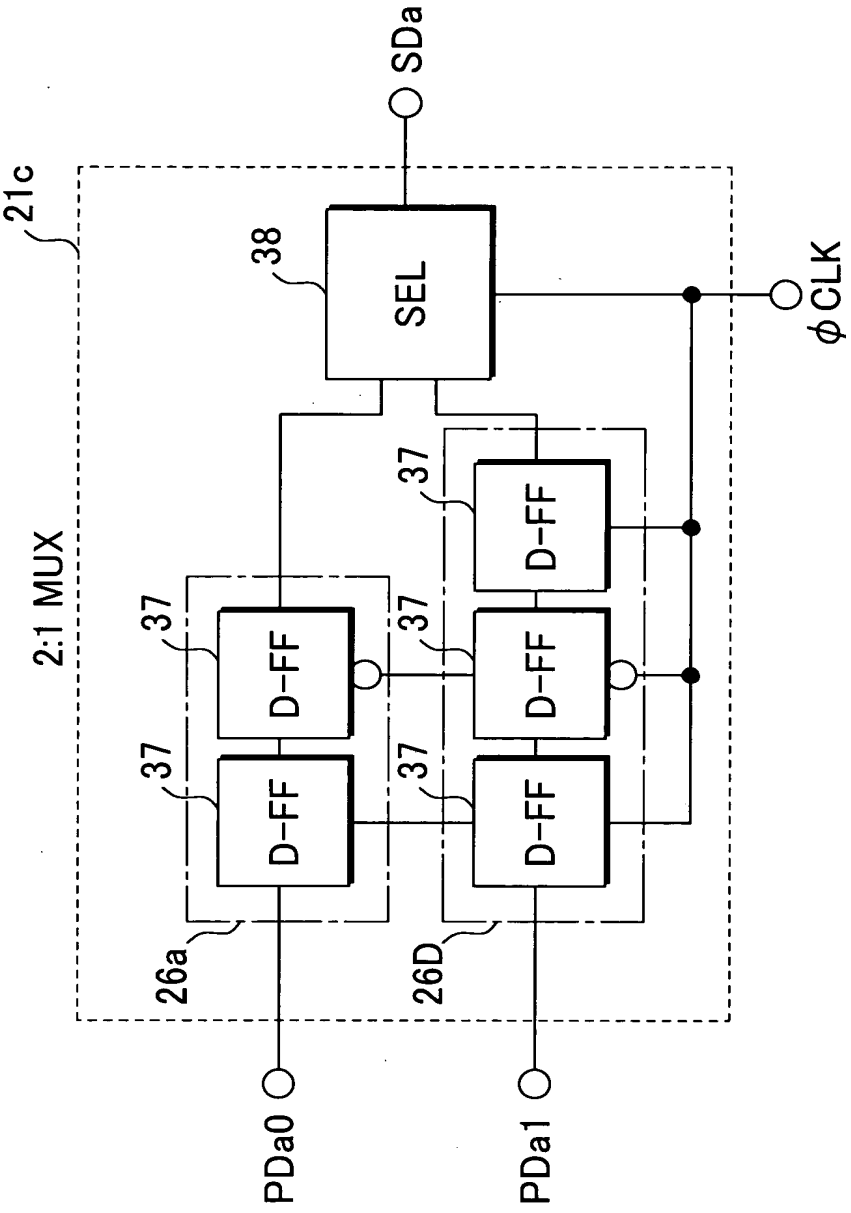

SDa
21c
38
SEL
φCLK
2:1 MUX
37
D-FF
37
D-FF
37
D-FF
37
D-FF
37
D-FF
37
D-FF
26a
26D
PDa0
PDa1

FIG.8

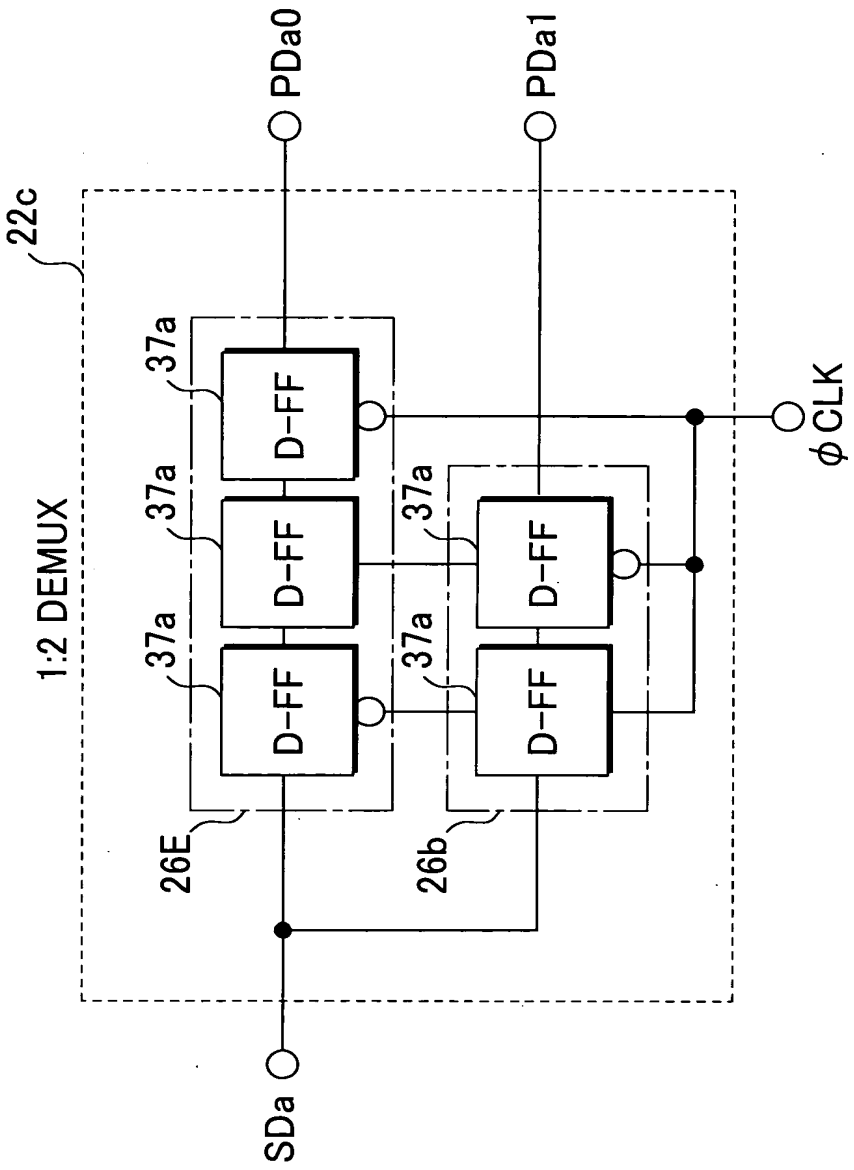

PDa0
PDa1
22c
1:2 DEMUX
37a
D-FF
37a
D-FF
37a
D-FF
37a
D-FF
37a
D-FF
φCLK
26E
26b
SDa

FIG.9

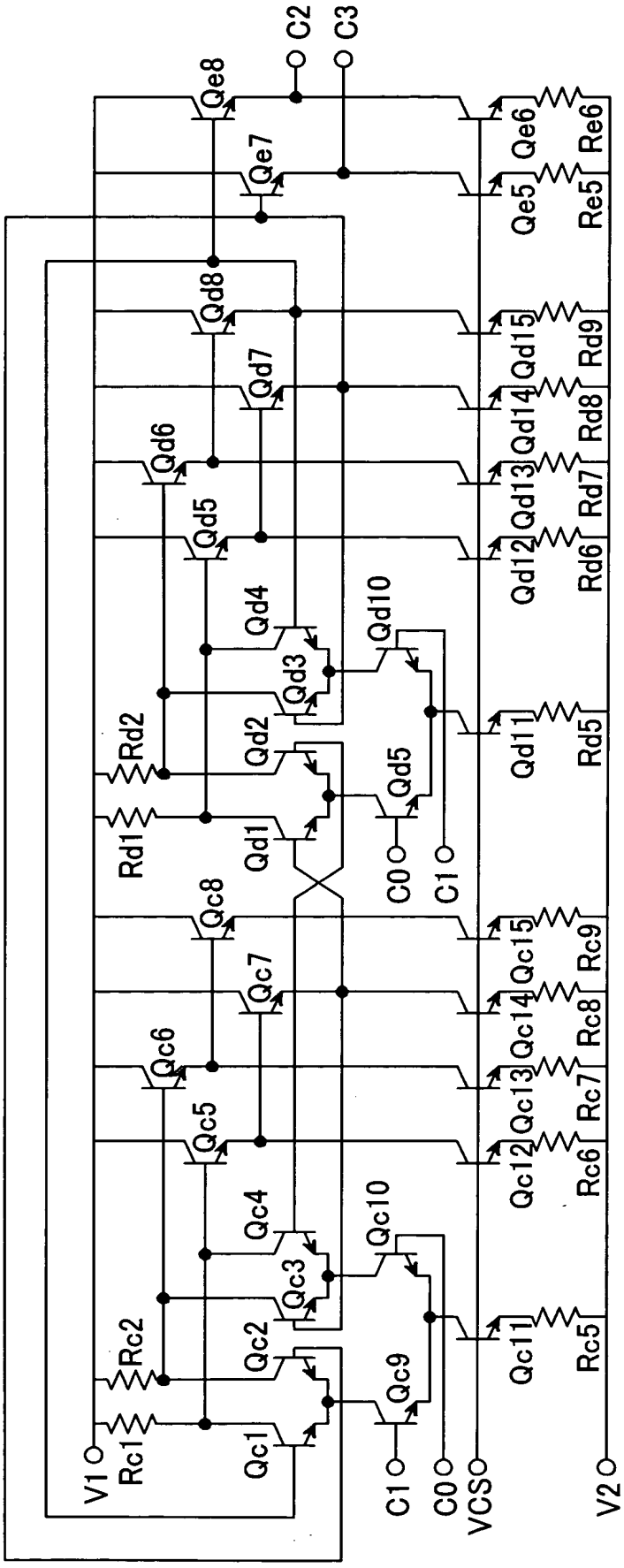

C2
C3
Qe8
Qe7
Qe6
Re6
Qe5
Re5
Qd8
Qd7
Qd6
Qd5
Qd4
Qd3
Qd2
Qd1
Qd10
Qd5
Qd15
Qd14
Qd13
Qd12
Qd11
Rd9
Rd8
Rd7
Rd6
Rd5
Rd2
Rd1
C0
C1
Qc8
Qc7
Qc6
Qc5
Qc4
Qc3
Qc2
Qc1
Qc10
Qc9
Qc15
Qc14
Qc13
Qc12
Qc11
Rc9
Rc8
Rc7
Rc6
Rc5
Rc2
Rc1
V1
C1
C0
VCS
V2

FIG.10

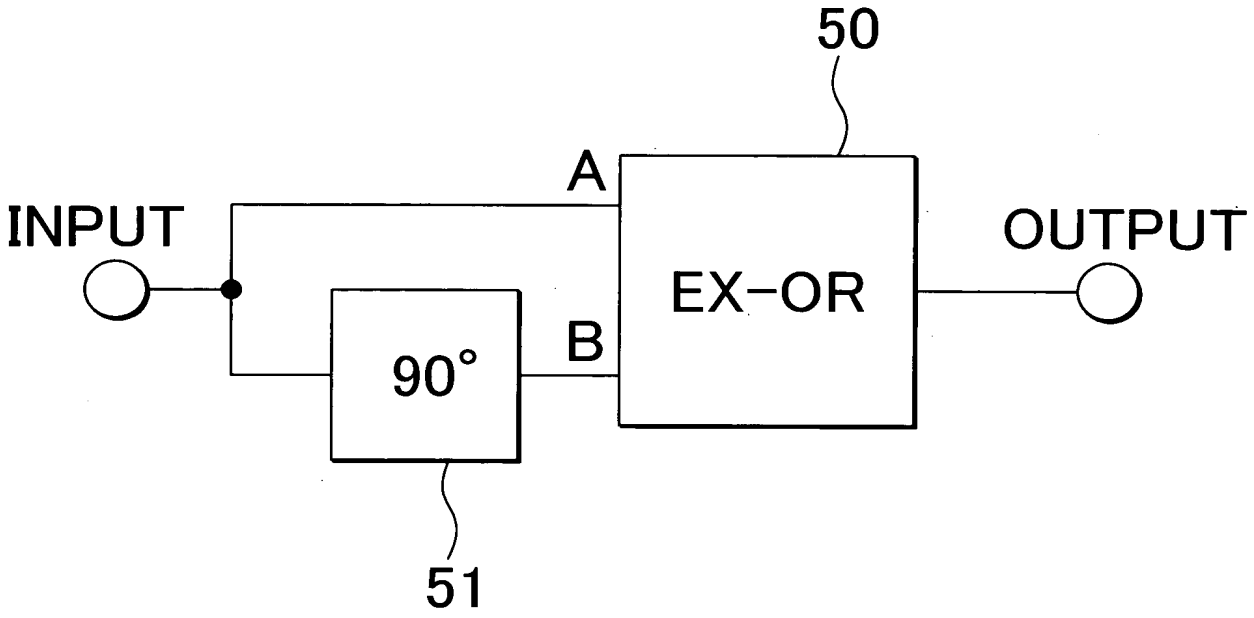

50
A
INPUT
OUTPUT
EX-OR
90°
B
51

FIG.11

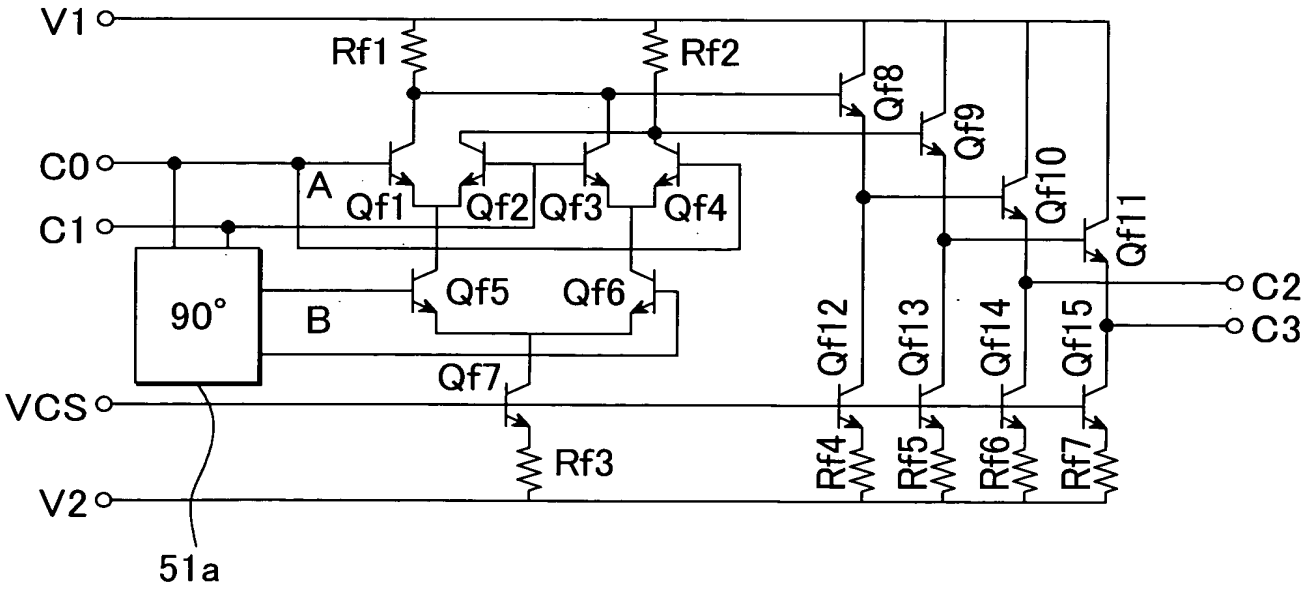

V1
Rf1
Rf2
Qf8
Qf9
Qf10
Qf11
C0
A
Qf1
Qf2
Qf3
Qf4
C1
C2
C3
90°
B
Qf5
Qf6
Qf7
Qf12
Qf13
Qf14
Qf15
VCS
Rf3
Rf4
Rf5
Rf6
Rf7
V2
51a

FIG.12

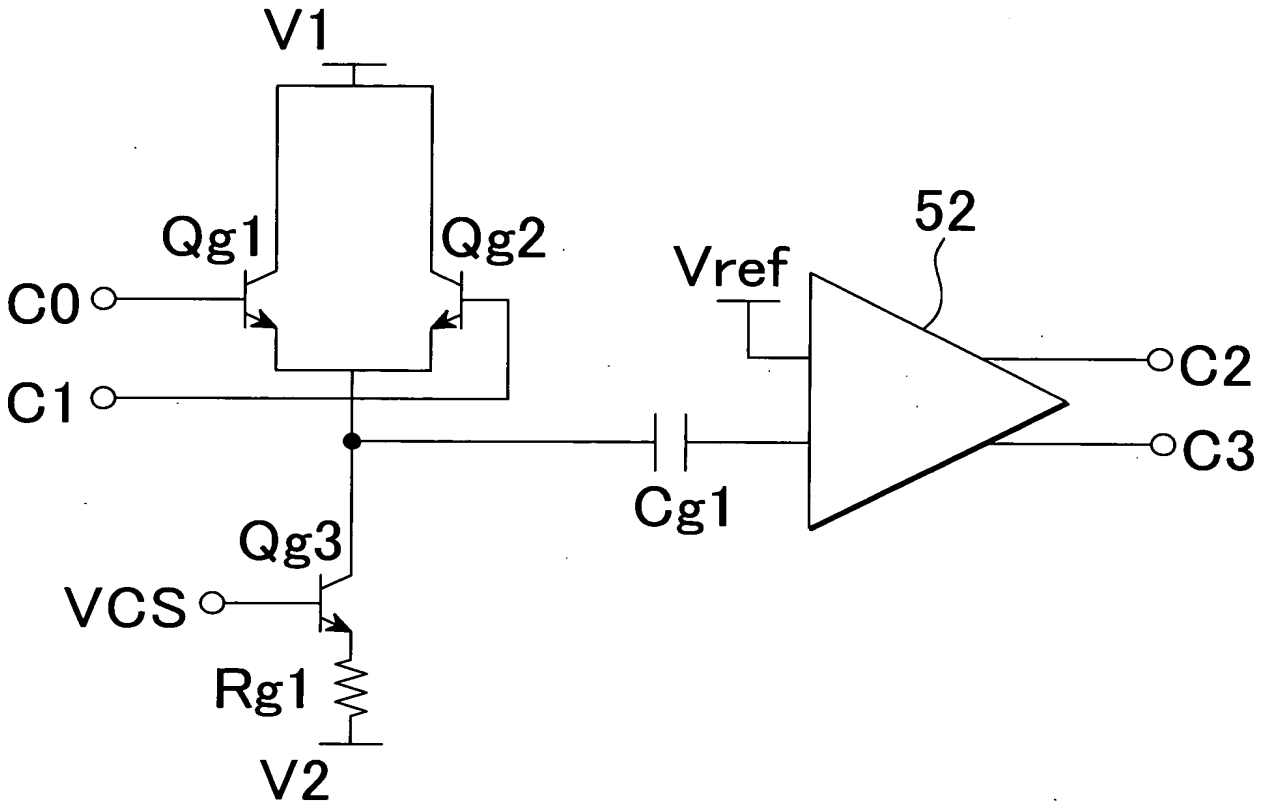
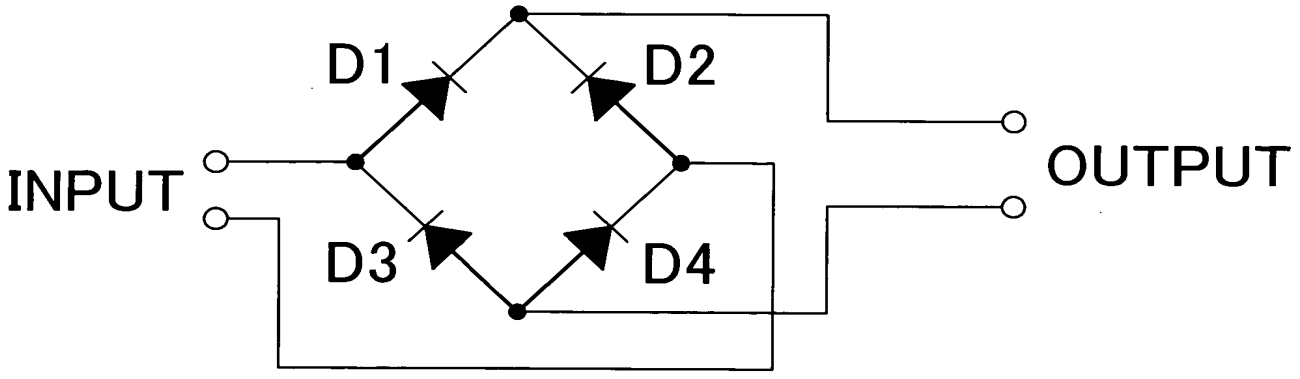

V1
Qg1
Qg2
52
Vref
C0
C1
C2
C3
Cg1
Qg3
VCS
Rg1
V2

FIG.13


D1
D2
INPUT
OUTPUT
D3
D4